CHAPTER 29

LIMITERS AND AUTOMATIC FREQUENCY CONTROL

By B. SANDEL, A.S.T.C.

Section Page

SECTION 1 : LIMITERS

(i) General (ii) Typical circuits for F-M receivers (a) Single stage limiter (b) Cascaded limiters.

(i) General

In this section it is proposed to discuss only the conventional type of amplitude limiter using a pentode valve operating as a saturated amplifier. Other circuits, which combine the dual functions of detection and the removal of amplitude variations, such as the ratio detector and locked oscillator, will not be treated here. The ratio detector has been discussed in detail in Chapter 27 Sect. 2. Details of several other alternative systems can be found in Refs. 2, 5, 6, 7 and those at the end of Chapter 27.

The need for some form of amplitude limiting was stressed in Chapter 27 Sect. 2, when the phase discriminator was being discussed. It was pointed out that the diodes in a phase discriminator are amplitude modulation detectors, and if undesired amplitude variations are not to appear in the receiver output the amplitude of the voltage applied to the discriminator should be constant. This was emphasised by reference to eqns. (20) and (21), where it was seen that the product $g_m E_g$ should be held constant if the discriminator sensitivity is to remain fixed for a given frequency deviation.

Circuit arrangements for limiters in F-M broadcast receivers have become quite stereotyped. Sharp cut-off pentodes having fairly high values of g_m are the usual choice, and typical of these are types 6SJ7, 6SH7 and 6AU6. The limiting action is brought about by a combination of grid-leak bias and low values of plate and screen voltage. Grid-bias limiting is obtained by adding a resistor and capacitor, of suitable value, to the grid circuit and using zero or very small values of cathode bias. The grid circuit arrangement is the same as for a grid-leak detector, and the operation is almost identical since the average negative bias on the grid is determined by the $e_g - i_g$ characteristics of the valve in conjunction with the associated circuit. The value of the average grid bias, together with the low screen voltage, determine the condition for which plate current cut-off occurs. Any signal input voltage whose amplitude is sufficiently large will cause the average negative bias to increase and so tend to hold the output voltage constant. Because of the low values of plate and screen voltage the plate voltage swing is limited to a comparatively small value and, for an input signal of sufficient magnitude, there will be practically no corresponding increase in output voltage when the signal input voltage is increased.

The added damping on the i-f transformer secondary, which connects to the limiter grid, is given approximately by $R_g/2$ or $R_g/3$, depending on the circuit arrangement, in exactly the same way as discussed previously for a diode detector ; R_g being the value of resistance selected for the grid leak. This should be taken into account (as well as circuit detuning caused by changes in the valve input capacitance) when the i-f transformer is being designed.

The necessity for high gain in the receiver stages preceding the limiter stage will be appreciated when it is realized that a minimum of about 2 volts peak is required at the limiter grid to obtain satisfactory operation with a typical circuit arrangement ; it is preferable to have voltages of the order of 10 to 20 volts peak for best results under adverse condition of reception. Since this limiter input voltage must be obtained with the smallest signal input voltage likely to be met in the field, the gain of the preceding stages in the receiver should be sufficient to give satisfactory limiter operation with signal voltages as low as 2 or 3 μV ; in F-M mobile communications applications the limiter should saturate with signals of less than 1 μV. Also, because the conversion from F-M to A-M in the discriminator usually results in a low equivalent value of percentage amplitude modulation, it is necessary for the limiter output voltage to be large if the detected audio voltage is to be sufficient to drive the audio amplifier to full output ; this means that something in excess of 10 volts peak is desirable at the plate circuit of the limiter.

For completely satisfactory amplitude limitation two limiter stages are necessary. However, because of the cost factor, commercial domestic type receivers seldom use more than one limiter stage. When two stages of limiting are used, it is essential that the coupling circuit between them should not introduce any appreciable amplitude modulation due to its selectivity characteristic. The selectivity should be sufficient to attenuate harmonics of the intermediate frequency generated by the limiter, although this is also accomplished by the primary of the discriminator transformer ; with single stage limiters the discriminator transformer is relied upon to give the necessary attenuation of the i-f harmonics. Transformer coupling between the two limiter valves is the most satisfactory arrangement, but single tuned circuits are often used.

The choice of the time constant for the grid resistance-capacitance combination is important. It must be sufficiently short for the grid bias to be proportional to changes in amplitude, but not so short as to prevent the bias change from being sufficiently large to control the amplification of the limiter stage, so as to offset any change in signal input voltage. For a single stage, limiter time constants of 2.5 microseconds are usual, although 10 to 20 microseconds and even higher have been used in some receivers. For two stages the first limiter grid circuit uses a time constant of 1.25 to 5 microseconds and 2.5 to 10 microseconds or longer in the second stage, in typical cases. The longer time constants of 10 to 20 microseconds are suitable for most types of noise impulses, but some forms of motor car ignition noise are more completely suppressed when the shorter time constants are used. A careful choice of the time constants is necessary if the noise is not to be heard in the receiver output because the bias on the limiter valve must be able to follow the changes in the amplitude of the input voltage.

No matter how effective the amplitude limiters may be and how carefully their time constants are chosen it will often be found that the F-M receiver will not effectively suppress bursts of noise such as those emitted by car ignition systems. To obtain the best results it is most important that the pass band of the receiver be symmetrical and that the centre frequency of the i-f amplifier coincides exactly with the centre frequency of the discriminator. A useful test is to align the receiver on an unmodulated carrier at the signal frequency and then to switch off the carrier ; if the alignment is correct, and the circuits symmetrical, a d.c. vacuum tube voltmeter connected across the discriminator output will give a reading of approximately zero (of course the usual noise will be heard from the receiver output). Small inaccuracies often arise when the receiver is aligned so as to give maximum grid current at the limiter stage, or stages, even though the signal (unmodulated carrier) frequency is such that zero d.c. output voltage is obtained from the discriminator. The grid current reading is usually rather broad, and it will be found that the i-f and limiter circuits, in particular, can often be realigned to give zero d.c. output voltage at the discriminator on noise without reducing the limiter grid current on signals. As a further check on alignment and symmetry the receiver is tuned very carefully to an unmodulated carrier so that the a.c. voltage at the output transformer is a minimum (i.e. for maximum quieting) and for this condition the reading of the d.c. voltmeter at the discriminator is noted ; then it will usually be found that this latter reading is the same as that obtained from noise alone. (A casual reading of the text may not bring out the full significance of this test, but a practical trial will lead to a better appreciation of its possibilities). If minimum noise output, zero d.c. discriminator output voltage, and maximum limiter grid current do not all occur at the same carrier frequency, then in general the optimum conditions for impulse noise rejection have not been obtained.

For applications other than domestic receivers the above factors require very careful attention.

(ii) Typical circuits for F-M receivers

(a) Single stage limiter

A typical single stage limiter is shown in Fig. 29.1, and an alternative arrangement is shown for the input circuit in Fig. 29.2. The time constant for R_gC_g is 2.5 microseconds in each case.

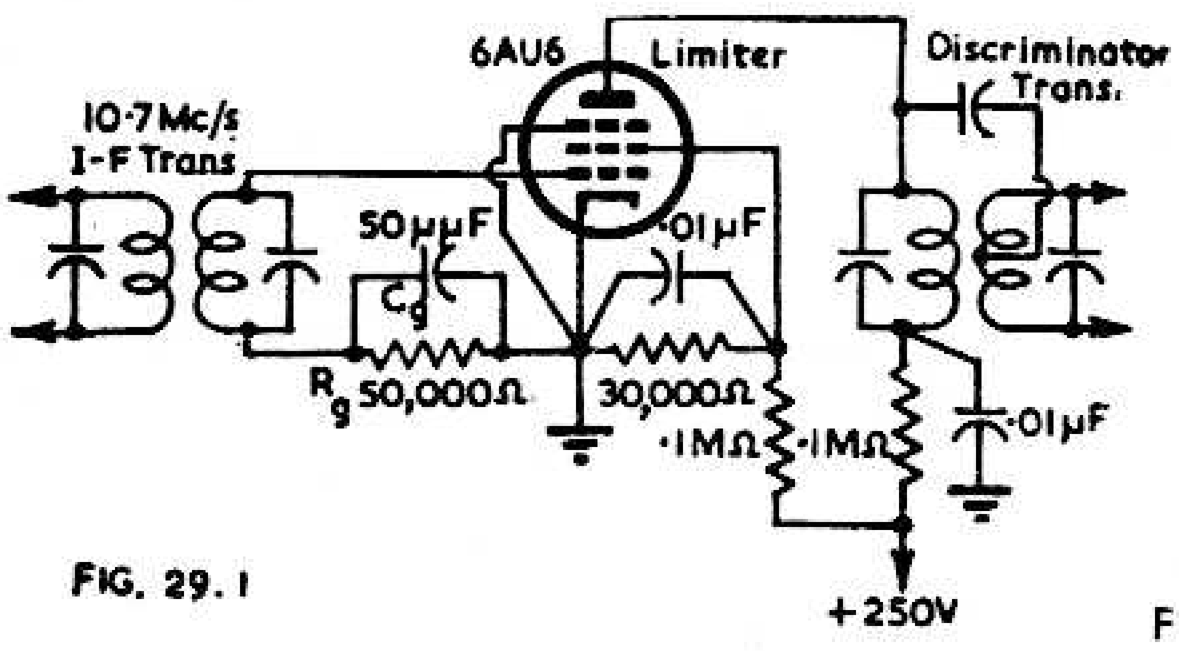

FIG. 29.1

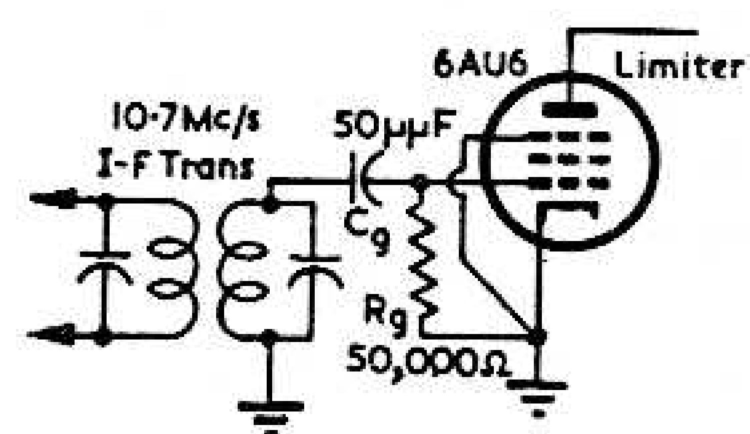

FIG. 29.2

The operation of both circuits is identical, but the damping of the i-f transformer due to grid current is less with the arrangement of Fig. 29.1, being approximately 50 000/2 = 25 000 ohms. The damping in the alternative arrangement is 50 000/3 = 16 600 ohms. Whichever circuit is used will depend, largely, on the additional damping required on the transformer to achieve the required bandwidth or, perhaps, upon considerations of practical convenience. The general method of operation has been discussed in (i) above.

If complete valve characteristics are available then a preliminary design can be made, but the work involved is hardly worth the effort because of the ease with which the practical circuit can be made to give satisfactory results using experimental procedures. For a calculation of gain, or overall discriminator sensitivity, it is necessary to determine the mutual conductance under the actual operating conditions. This can usually be determined, with sufficient accuracy for a preliminary design, from the valve data sheets by ignoring the change in plate voltage (provided the change in plate current with plate voltage does not fall too far down on the knee of the plate characteristics). For example, a type 6AU6 is to be operated with 50 volts on the plate and screen, and zero grid bias. From the average characteristics relating grid No. 1 volts to transconductance, the g_m is 4000 micromhos for zero bias, 50 volts on the screen and 250 volts on the plate. For typical cases of the type being considered, the g_m so found is usually about 10% high, and so 3600 micromhos would be a closer approximation. Alternatively, the valve can be set up as a straight amplifier with the appropriate d.c. voltages applied, and a 1000 ohm resistor connected as the plate load. Then with 1 volt of a-f input (from a source of low d.c. resistance) the output voltage will equal the g_m in mA/volt ; the actual input voltage is selected so that the stage just starts to saturate. However, overall measurements of actual circuit performance are preferable.

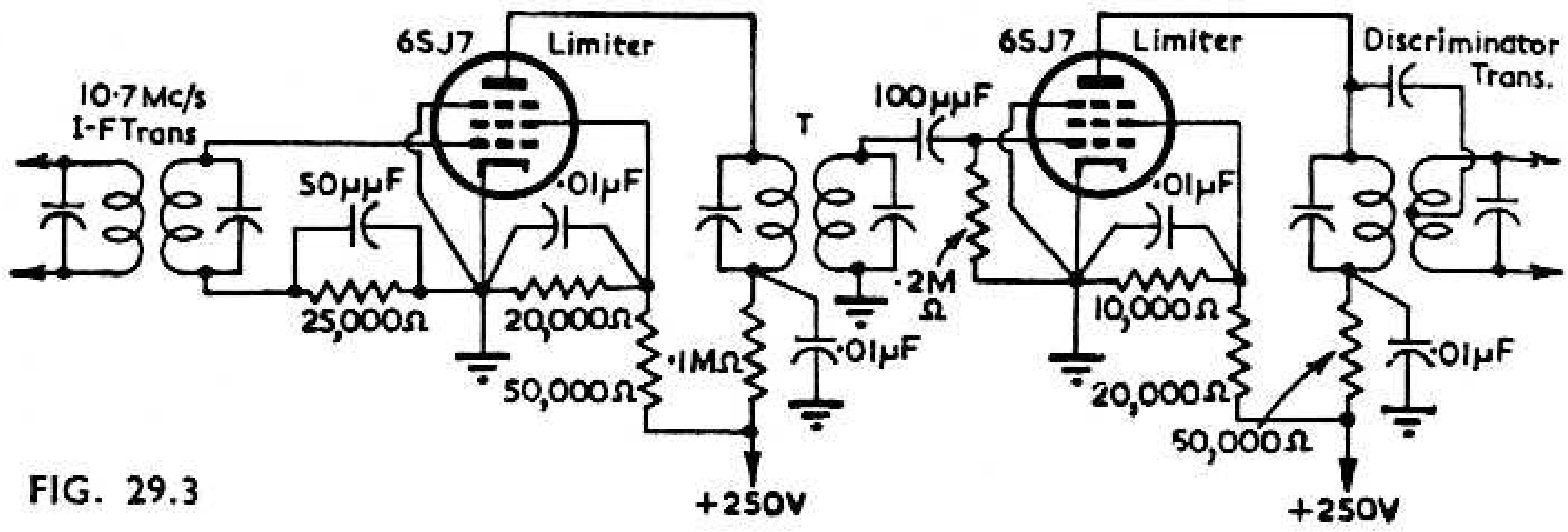

FIG. 29.3

(b) Cascaded limiters

A typical circuit for a two stage (cascaded) limiter is shown in Fig. 29.3. In this case the time constant of the grid resistance-capacitance combination is 1.25 microseconds for the first stage, and 20 microseconds for the second stage.

It should be noted that the limiters not only have to remove peaks of noise, but they must also remove the amplitude modulation introduced onto the frequency modulated signal by the receiver circuits which precede the limiters. Methods for estimating the percentage amplitude modulation introduced by tuned circuits are given in Chapter 26 Sect. 4. It will be realized that A-M introduced by the receiver itself makes it more difficult to effectively remove A-M introduced by external noise voltage sources.

For the transformer *T*, shown in Fig. 29.3, coupling the two limiter stages, it is essential that the amplitude modulation introduced by its selectivity characteristic should be as small as possible. However, its selectivity characteristic is helpful in removing harmonics of the i-f generated by the limiter, and so a practical compromise between the two conflicting factors is necessary. A critically-coupled transformer is recommended, and the primary and secondary *Q*'s (uncoupled) can be about 30 for an i-f of 10.7 Mc/s. The stage gain will be roughly 6 times depending on the circuits constants selected, and the magnitude of the input voltage.

From the circuit arrangements of Figs. 29.1 and 29.3 it will be noticed that the screen voltage is supplied from a voltage divider in each case. This arrangement is recommended in all cases, but in mobile communications receivers it will be found that many circuits use only a series screen resistor ; the main advantage of this latter arrangement is economy in the total H.T. current drawn by the receiver.

SECTION 2 : AUTOMATIC FREQUENCY CONTROL

(*i*) *General principles* (*ii*) *Discriminators for a.f.c.* (*iii*) *Electronic reactances.*

(i) General principles

Although the description given below of automatic frequency control (a.f.c.) systems is confined to simple applications in broadcast receivers, it should not be overlooked that the same general principles are applied in many other types of equipment and are used, for example, to obtain frequency stabilization in F-M transmitters, microwave radar receivers and transmitters etc.

Automatic frequency control in a superheterodyne radio receiver is an arrangement for controlling the local oscillator frequency in such a way that, when a signal is being received the correct intermediate frequency will be produced. For example, if a receiver is manually tuned so that it is, say, 3 Kc/s away from a desired signal the oscillator frequency will be varied by the a.f.c. system so as to produce the correct intermediate frequency (or at least within 100 c/s or so of the correct value, since exact compensation is not possible). Alternatively, the oscillator frequency may drift because of temperature or humidity variations affecting the values of the circuit components, and a.f.c. will tend to compensate for this frequency variation. However, the frequency stability of the receiver should be made as good as possible without relying on the a.f.c. system.

The most useful application of the system in broadcast receivers is with those receivers having automatic tuning e.g. push-button station selection, and cam or motor driven variable capacitors. In cases of this type the tuning may not be accurate over extended periods of time, and a.f.c. may be used effectively to carry out the final adjustment when the respective capacitances and/or inductances have been selected by the automatic tuning system.

There are two devices necessary for any a.f.c. system. These are :—

(1) A frequency discriminator, which must be capable of changing a frequency variation into a suitable direct voltage change which can be used for control purposes.

(2) A variable reactance, whose value can be controlled by the direct voltage changes due to the frequency discriminator. The variable reactance is connected to the oscillator circuit in such a way as to control its frequency.

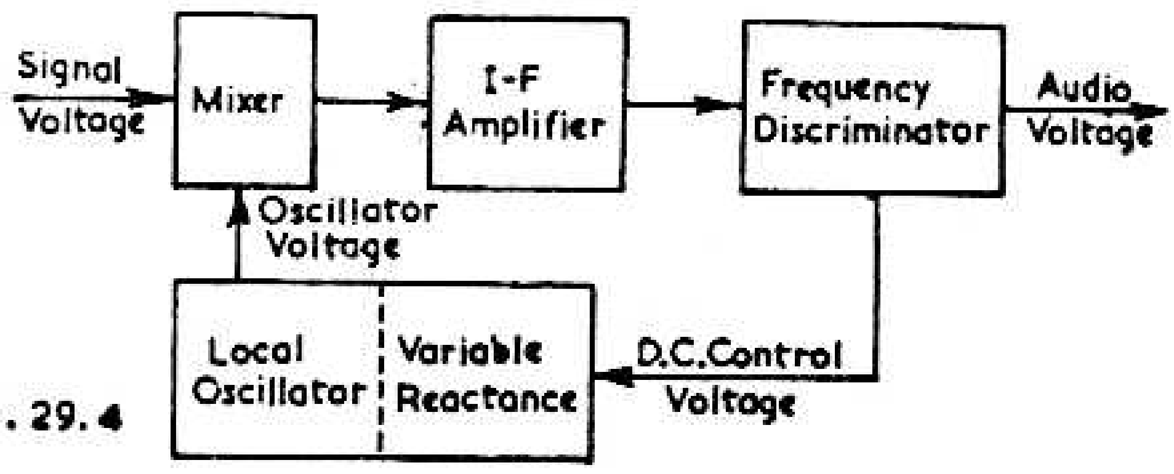

FIG. 29.4

The complete arrangement can be visualized with the aid of the block schematic of Fig. 29.4. It is seen that the additional elements to those normally found in a superheterodyne receiver are the frequency discriminator and the variable reactance. The variable reactance in the discussion to follow will be of the electronic type consisting of a valve (which can be a pentode, a hexode or a heptode) and its associated circuits. It will also be inferred from Fig. 29.4 that the frequency discriminator can be used for normal detection, since there are suitable audio voltages developed in this circuit by the applied modulated i.f. voltage.

Suitable voltages for a.v.c. are also available from the discriminator output, but in this regard it is necessary to point out that a very efficient a.v.c. system is helpful in obtaining satisfactory operation from the a.f.c. system. If reasonably constant input voltage to the discriminator is not maintained, there will be a variation in the " pull-in " and " throw-out " frequencies. Because of the stringent a.v.c. requirements it is fairly common practice to employ a separate diode coupled to the transformer primary, in the usual manner, to provide the a.v.c. bias voltage. There is also a disadvantage in taking the a-f voltage from the discriminator output as the distortion tends to be fairly high. However, in most commercial receivers the cost factor leads to some arrangement such as that of Fig. 29.8.

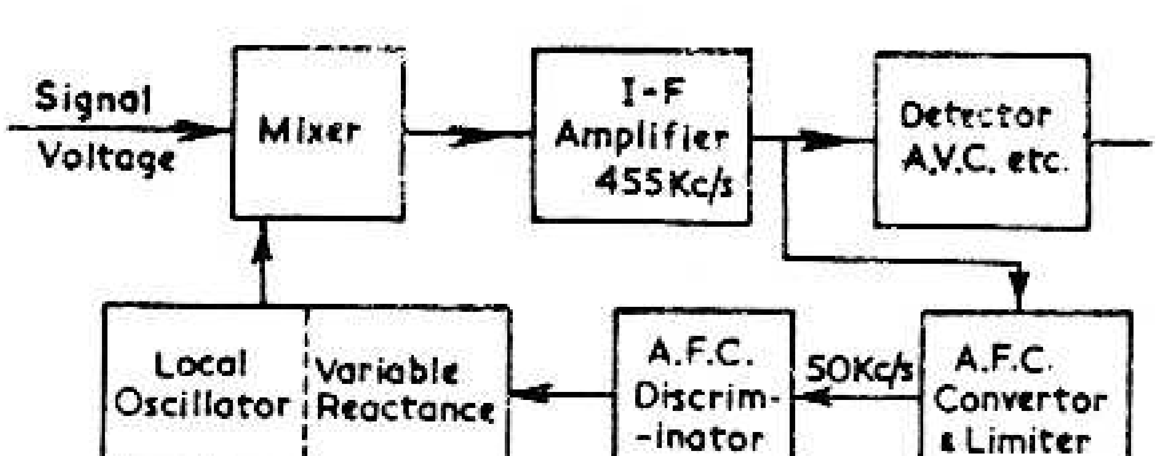

FIG. 29.5

A much more satisfactory method (although considerably more expensive) of obtaining a.f.c. is illustrated by the block schematic of Fig. 29.5. In this case the valve used as an a.f.c. converter and limiter is loosely coupled to the primary of the last i-f transformer. The 455 Kc/s signal is converted to 50 Kc/s to operate the a.f.c. discriminator, and the d.c. output voltage then controls the variable reactance in the usual manner. The use of limiting is helpful in maintaining a constant amplitude for the voltage to be applied to the discriminator. It will also be noticed that the functions of detection and a.v.c. have been separated from the a.f.c. system. A complete circuit using this arrangement can be found in Ref. 15 (page 103), together with a number of other commercial a.f.c. circuits of various types.

(ii) Discriminators for a.f.c.

The function of the frequency discriminator in an automatic frequency control system is to provide a suitable direct controlling voltage for application to the electronic reactance. When the receiver is tuned exactly to the signal frequency, the voltage output from the discriminator should be zero, or else have the same value as that provided in the absence of a signal, so that the controlled reactance will have its normal value. At frequencies above and below the correct frequency the controlling voltage should be appropriately above and below the mean voltage. The operation in connection with a phase discriminator has been discussed in Chapter 27 Sect. 2. The manner in which the output voltage will vary with the frequency change for either the amplitude or the phase discriminator can be seen from Fig. 29.6.

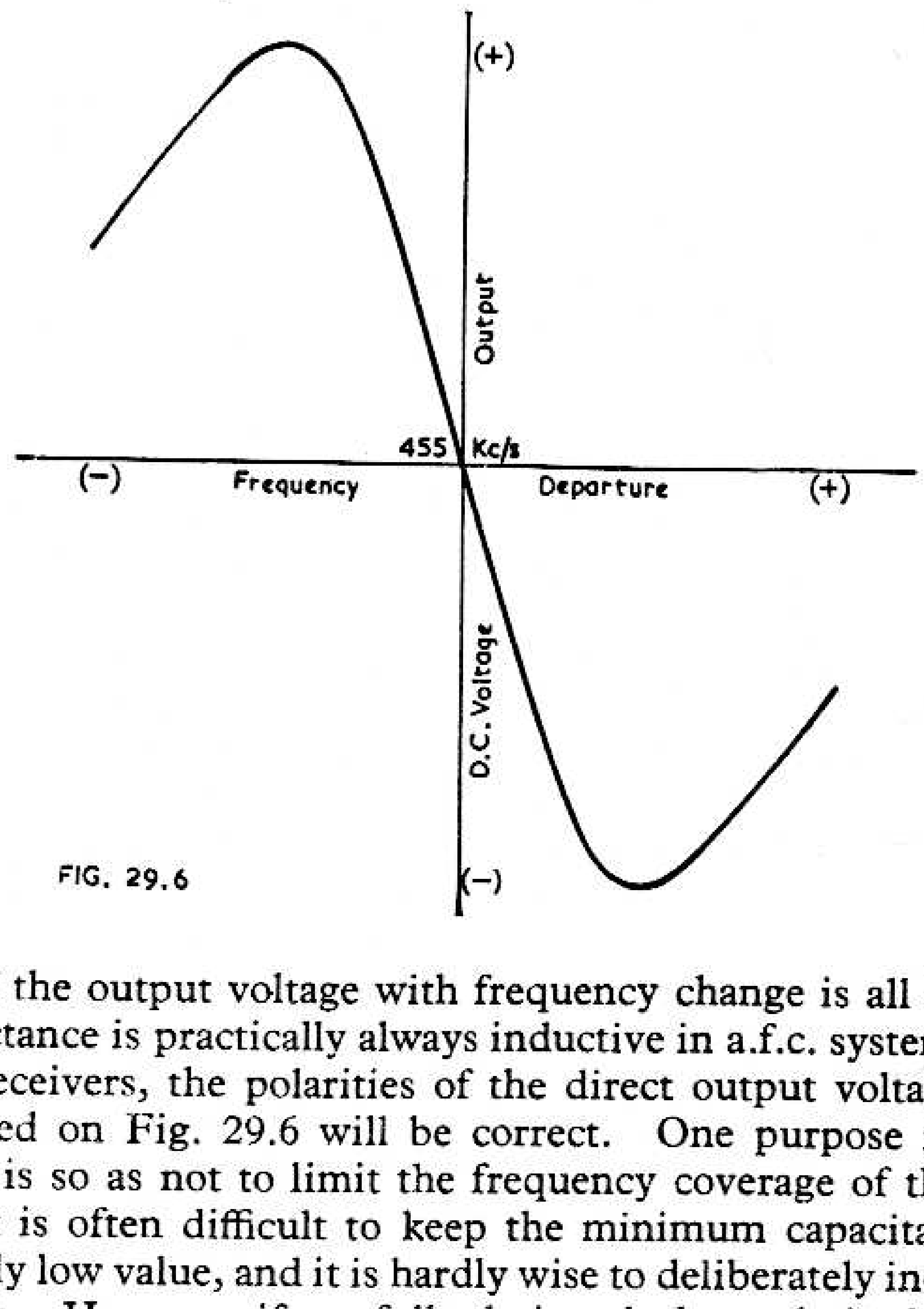

FIG. 29.6

The polarity of the output voltage with frequency change is all important, and, as the electronic reactance is practically always inductive in a.f.c. systems used in tunable broadcast radio receivers, the polarities of the direct output voltage with frequency change as indicated on Fig. 29.6 will be correct. One purpose in making the reactance inductive is so as not to limit the frequency coverage of the receiver. This follows because it is often difficult to keep the minimum capacitance of the tuning unit to a sufficiently low value, and it is hardly wise to deliberately increase this capacitance unnecessarily. However, if carefully designed, the undesired added capacitance due to the capacitive reactance unit can be made very small.

The effect of the added parallel inductance can usually be offset fairly readily by increasing the inductance of the oscillator coil. With receivers using push-button tuning where the circuits are of the preset type either the inductive or capacitive form of electronic reactance is satisfactory. For receivers with inductance tuning a capacitive electronic reactance is usually preferable. The degree of frequency correction is not constant over a band of frequencies, and this again suggests an inductive electronic reactance when the circuits are tuned by a variable capacitor, since the least error is obtained at the low frequency end of the tuning range where the receiver is most selective.

It may be helpful to follow through the steps leading to the polarities shown for the direct voltage with frequency change. Suppose the receiver is tuned to a signal of 1500 Kc/s. Then the oscillator will be set at 1955 Kc/s to give an i-f of 455 Kc/s, and there will be no direct voltage output from the discriminator. If now the oscillator drifts to 1957 Kc/s the i-f produced will be 457 Kc/s, and a direct voltage of negative polarity will be produced by the discriminator and applied to the reactance valve. The equivalent inductance of the electronic reactance is inversely proportional to mutual conductance (g_m) and so, as a more negative bias voltage reduces g_m, the shunt inductance across the oscillator coil is increased, the **total** inductance in the oscillator circuit is now increased, thus lowering the oscillator frequency as required.

The two most commonly used types of discriminator circuits are shown in Figs. 29.7 and 29.8. The first is generally known as the Round-Travis circuit (see Ref. 10), and is a typical example of an amplitude discriminator. The secondary circuits A and B are so tuned that A has its resonant frequency slightly above the intermediate frequency and B is set slightly below the i-f (say +5 Kc/s in one case and −5 Kc/s in the other). Each secondary circuit has its own diode detector and the diode loads are connected in d.c. opposition, so that when the i-f is greater than the required value of 455 Kc/s (and since the voltages developed across R_1 and R_2 have the polarities shown) the voltage across R_1 is greater than that across R_2 and the a.f.c. bias voltage is negative as is required for correction of the oscillator frequency. For example, the voltage across R_1 may be 4 volts when that across R_2 is 3 volts, then the available a.f.c. bias is −1 volt.

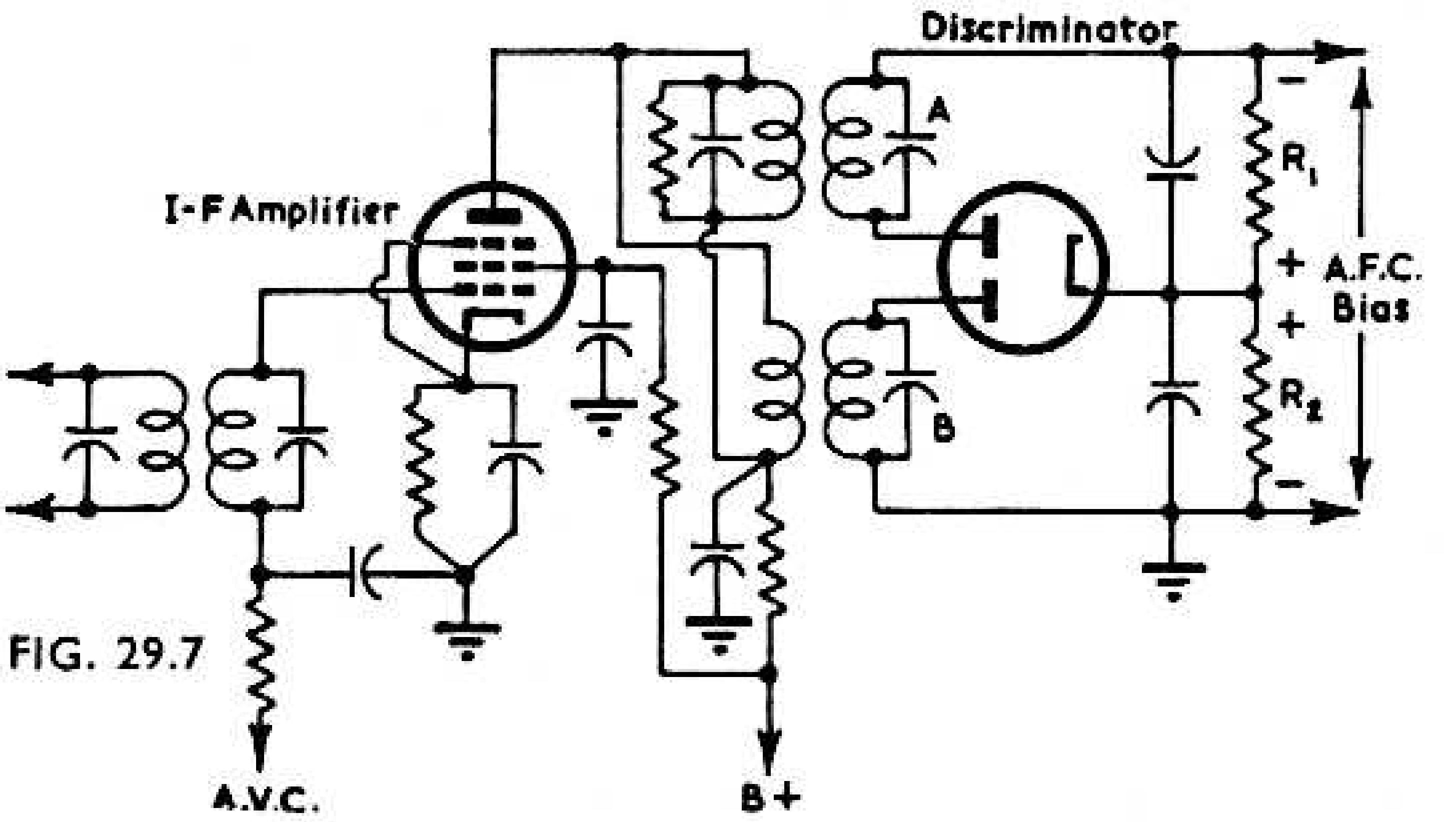

FIG. 29.7

The design procedure for an amplitude discriminator for a.f.c. is set out in detail in Ref. 8. Since this type of circuit is seldom used in modern a.f.c. systems the details of its operation will not be discussed further. There are a number of alternative arrangements for the amplitude discriminator, and some of these are discussed in Refs. 8, 9, 11, 15 and 13. It will be appreciated that a circuit of this type could be used for F-M detection as an alternative to the phase discriminator, and several manufacturers have produced F-M receivers using modified amplitude discriminators (see Ref. 39 given at end of Chapter 27, for typical examples).

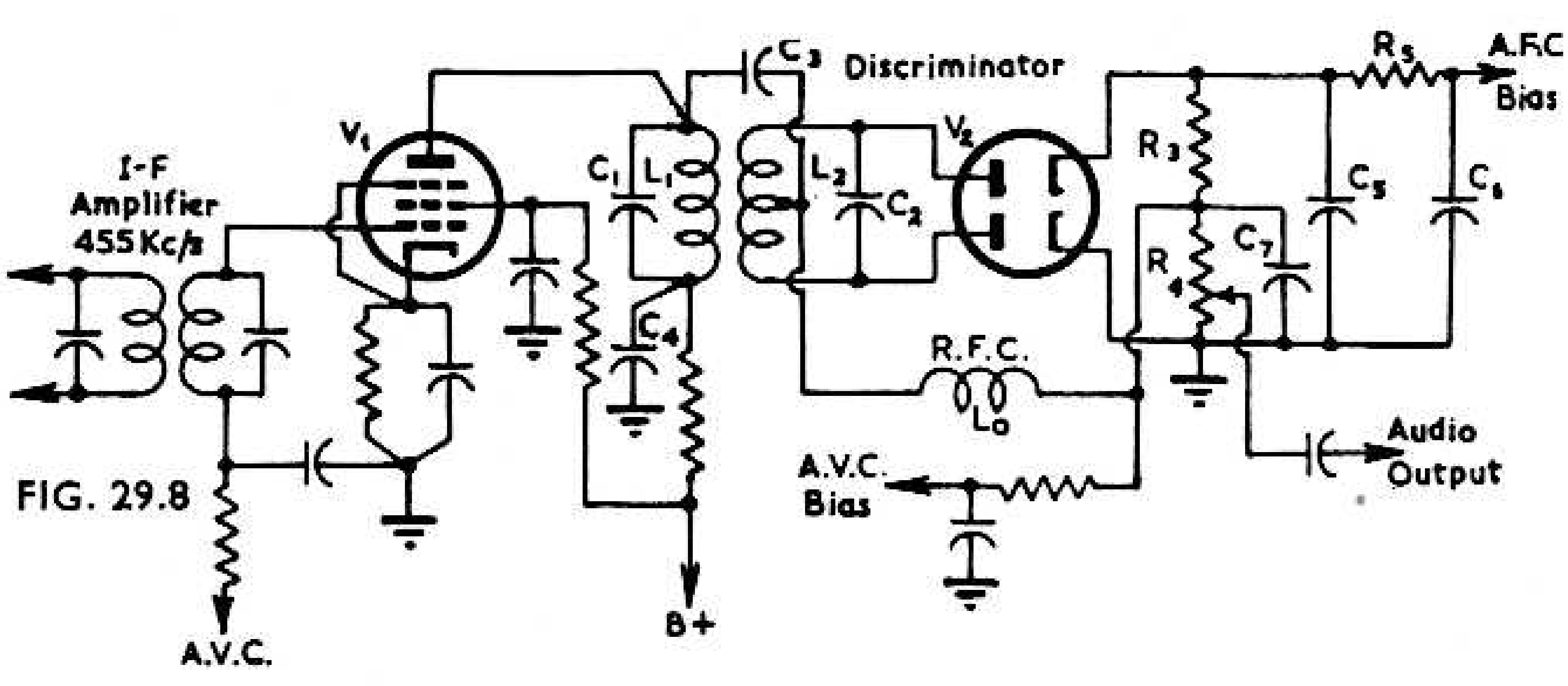

FIG. 29.8

Fig. 29.8 shows the most commonly used circuit, the phase (or Foster-Seeley) discriminator. In this circuit both primary and secondary circuits are tuned to the intermediate frequency. It will be seen that the circuit arrangement is identical with that of the F-M phase discriminator shown in Fig. 27.19, and the general discussion of its operation and the loading effects on the transformer apply equally well here. The de-emphasis circuit is not required here, of course, but the same general arrangements can be retained to provide r-f and a-f filtering, since only a direct control voltage is required. Suitable values for the filter circuit are R_5 equal to 0.5 − 2 MΩ, and C_6 is, say, 0.05 − 0.1 μF. The considerations governing the choice of the component values can be compared with those for selecting filter components for automatic volume control circuits, and a time constant for R_5C_6 of about 0.1 second is usual. The circuit arrangement of Fig. 27.17 could also be used here, and, if the primary circuit is too heavily damped, an additional series resistor can be inserted between the transformer centre-tap and the junction of the diode load resistors R_3 and R_4; however, this will lead to some loss in available output voltage, depending on the value of series resistance selected. The difference in the by-pass capacitor arrangements (i.e. C_5 and C_7) for Figs. 27.17 and 27.19 (or Fig. 29.8) should be observed, and the discussion in Chapter 27 Sect. 2, in connection with Fig. 27.19 will be helpful, if the reasons for the arrangements are not immediately obvious. The considerations leading to the choice of actual circuit values will differ because the a.f.c. discriminator is usually designed for high sensitivity rather than for a very high degree of linearity.

The theory of the circuit for a.f.c. use has been discussed by Roder (Ref. 14) and design procedures have been treated in detail in Ref. 8. A brief discussion, which is quite helpful, is given in Ref. 13.

The method of obtaining a-f output and a.v.c. bias from the a.f.c. discriminator circuit is also shown in Fig. 29.8. To retain the same degree of selectivity as that obtained with a similar receiver not incorporating a.f.c. one extra tuned circuit is required. This is necessary because the discriminator provides very little selectivity as a result of the heavy loading effects produced by the diodes. There is some increase in gain over the usual arrangement where the a-f detector is connected across the i-f transformer secondary only.

The frequency at which the a.f.c. will come into operation when tuning a signal is called the "pull-in frequency." When tuning away from a carrier the frequency at which the a.f.c. loses control is called the "throw-out frequency," and it is always greater than the "pull-in frequency." It is desirable to make these two frequencies as close as possible, because stations which are received when tuning-in may be passed over when tuning-out. Many receivers incorporate arrangements for disconnecting the a.f.c. until a carrier has been approximately tuned-in (see Refs. 8, 15).

Some of the general details of the discriminator design will be set out here, and the reader is referred to Refs. 8, 9 and 14, in particular, for further information. Consider Fig. 29.8. Typical values for R_3 and R_4 are 0.5 MΩ. Capacitors C_5 and C_7 must give adequate by-passing at the intermediate frequency of 455 Kc/s, and suitable values would be 100 to 200 $\mu\mu$F. C_3 is usually 100 $\mu\mu$F. Values for R_5 and C_6 have been discussed previously. The valve V_1 is any of the usual voltage amplifier pentodes such as type 6SK7 etc., and V_2 is a double diode such as the types 6H6 or 6AL5. The next step is to select a suitable value for the inductance of the r-f choke.

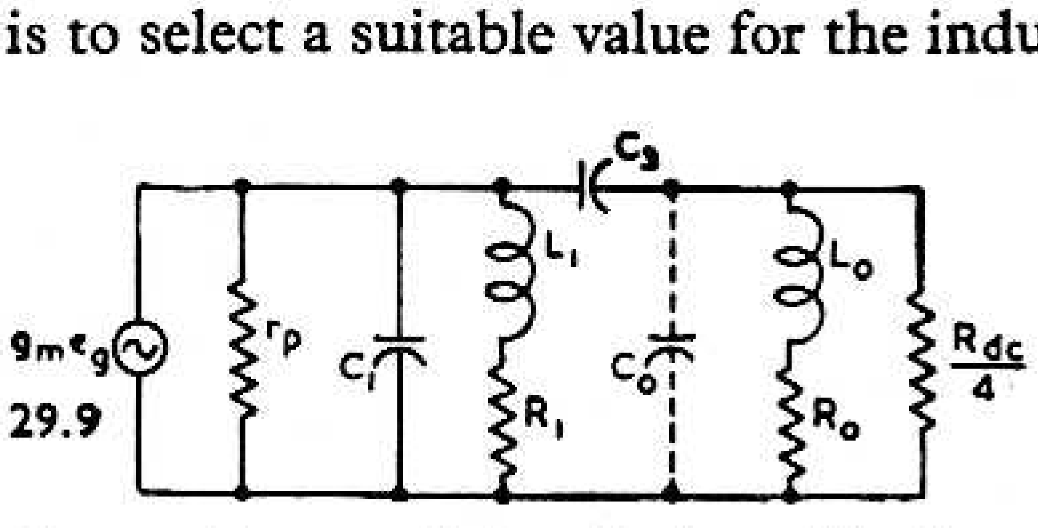

FIG. 29.9

As the inductance and capacitance of the choke will affect the resonant frequency of the transformer primary (L_1C_1) and its Q, care is necessary. The choke, in association with the transformer primary circuit, can be represented by the equivalent circuit of Fig. 29.9 in which $g_m e_g$ represents the equivalent constant current generator for the pentode voltage amplifier; r_p is the plate resistance; C_1 is the total primary capacitance including strays; L_1 is the primary inductance and R_1 its r-f resistance; C_3 is the capacitor connecting the plate circuit to the choke L_0 (whose r-f resistance is R_0); C_0 represents any distributed or stray capacitances across L_0; $R_{dc} = R_3 = R_4$ the diode load resistance. It should be apparent that three cases can arise with the choke (Ref. 14):—

(1) The capacitance C_0 negligibly small.
(2) The capacitance C_0 small enough to still allow the choke to be self resonant well above the intermediate frequency, but the value of C_0 to be such as to appreciably affect the resonant frequency of the complete primary circuit.

(3) The choke resonant at the intermediate frequency.

It follows from (1) and (2) that L_1 and C_1 should have a resultant capacitive reactance at the intermediate frequency, and in case (3) L_1 and C_1 should be resonant at the intermediate frequency.

Considering the above three cases in conjunction with Figs. 29.9 and 29.8, it can be seen that the derivation of the conditions for discriminator transformer primary resonance, voltage step down between the transformer primary and the choke, and the resultant Q's for the complete discriminator transformer, will follow fairly readily. The derivations are available in Ref. 14, and the results, which are good approximations, are summarized below (with some modifications, as well as changes in notation).

Case (1) (Choke capacitance C_0 negligibly small).

Condition for primary circuit resonance,

$$\frac{X_{L_0} - X_{C_3}}{X_{L_1}} = \frac{X_{C_1}}{X_{L_1} - X_{C_1}} \tag{1}$$

Voltage step down,

$$\alpha = 1 - \frac{X_{C_3}}{X_{L_0}} \tag{2}$$

Reciprocal of equivalent primary circuit Q (this leads to simpler numerical evaluation),

$$\frac{1}{Q_p} = \frac{1}{Q_0} + \frac{X_{L_0}}{R_{dc}/4} + \alpha^2 X_{L_0}\left(\frac{1}{Q_1 X_{L_1}} + \frac{1}{r_p}\right) \tag{3}$$

Secondary circuit Q (since the diode loading is R_{dc}) is

$$Q_s = \frac{Q_2 R_{dc}}{Q_2 X_2 + R_{dc}} \tag{4}$$

and this equation applies for the three cases—

where $X_{L_0} = \omega_0 L_0$ = inductive reactance of choke L_0

$X_{C_3} = 1/\omega_0 C_3$ = capacitive reactance of C_3

$X_{L_1} = \omega_0 L_1$ = inductive reactance of L_1

$X_{C_1} = 1/\omega_0 C_1$ = capacitive reactance of C_1

$\omega_0 = 2\pi \times$ intermediate frequency

Q_0 = magnification factor of choke L_0

Q_1 = magnification factor of L_1

$R_{dc} = R_3 = R_4$ = diode load resistance value

r_p = plate resistance of voltage amplifier valve

Q_2 = magnification factor of L_2

and $X_2 = \omega_0 L_2$ = inductive reactance of L_2.

Case (2) (Choke capacitance small but not negligible).

The angular resonant frequency of the choke is

$$\omega_r = 1/\sqrt{L_o C_o} \tag{5}$$

$$X'_{L_0} = X_{L_0}\left(\frac{\omega_r^2}{\omega_r^2 - \omega_0^2}\right) \tag{6}$$

$$Q'_0 = Q_0\left(1 - \frac{\omega_0}{\omega_r}\right)^2 \tag{7}$$

where C_0 = distributed capacitance of the choke, and all the other symbols are exactly as before.

Equations (6) and (7) are used directly with eqns. (1), (2) and (3) substituting X'_{L_0} for X_{L_0} and Q'_0 for Q_0.

Case (3) (Choke resonant at intermediate frequency).

The inductances L_1 and L_2 are connected in parallel, and α can be taken as unity (since X_{C_3} will be small, compared with the dynamic resistance of L_0C_0), so that the equivalent primary circuit reactance required to give parallel resonance is

$$X_p = \frac{X_{L_1} X_{L_0}}{X_{L_1} + X_{L_0}}. \tag{8}$$

The reciprocal of the equivalent loaded primary circuit Q is

$$\frac{1}{Q_p} = X_p \left[\frac{1}{Q_0 X_{L_0}} + \frac{1}{Q_1 X_{L_1}} + \frac{1}{r_p} + \frac{1}{R_{dc}/4} \right] \tag{9}$$

All notation exactly as for case (1).

It should be noted in all cases that the loaded Q's refer to the case where the primary and secondary are uncoupled from one another. This is the usual definition.

We are in a position to proceed with the determination of suitable values for the primary and secondary circuits of the discriminator transformer, since all the external effects can now be taken into account. What is required next are methods for determining optimum values for Q_p, Q_s, L_p and $L_s(= L_2)$ where these factors have the meanings given by eqns. (1), (3), (4) etc. and $L_s(= L_2)$ is the secondary inductance (since its value is not changed by the presence of the choke). If the choke is not used $X_{L_1} = X_{C_1} = X_p$ and so $L_1 = L_p$; the procedure is then as for any other phase discriminator. The design factors, as well as the bandwidth and sensitivity calculations given below, apply equally well for all phase discriminators provided the values of Q, L and k (coefficient of coupling) so determined are those actually obtained in the receiver.

Optimum values for $k\sqrt{Q_p Q_s}$ for various values of L_s/L_p [see Refs. (8) and (9)] can be found from

$$k(Q_p Q_s)^{\frac{1}{2}} = \left[\frac{(Q_p^2 Q_s^2 + 2 Q_p Q_s^3 L_s/L_p)^{\frac{1}{2}} - Q_p Q_s}{Q_s^2 L_s/L_p} \right]^{\frac{1}{2}} \tag{10}$$

Several values are listed below,

$L_s/L_p =$	1	2	4	6	
$Q_p/Q_s = 1/2$	0.786	0.707	0.625	0.578	$k(Q_pQ_s)^{\frac{1}{2}}$.
$Q_p/Q_s = 1$	0.856	0.785	0.707	0.657	
$Q_p/Q_s = 2$	0.909	0.855	0.786	0.740	

The sensitivity of the phase discriminator at the intermediate frequency (f_0) has been derived in Refs. (14) and (8). It is given by,

$$S = \frac{2 g_m Q_p X_p \eta Q_s^2 (L_s/L_p)^{\frac{1}{2}}}{f_0} \left[\frac{k}{(1 + Q_p Q_s k)^2 \left(1 + \dfrac{Q_s^2 k^2 L_s}{4 L_p}\right)^{\frac{1}{2}}} \right] \tag{11}$$

and is expressed in direct volts output per Kc/s off tune, for each 1 volt (peak) input to the i-f amplifier valve V_1 (Fig. 29.8).

The symbols are the same as those used previously, with the addition of g_m the mutual conductance of V_1, and η is the detection efficiency of the diodes V_2.

It is necessary to estimate the peak separation for the discriminator characteristic of Fig. 29.6. This can be found (Ref. 8) from,

$$2\Delta f = \frac{f_0}{Q_s} \tan \phi \tag{12}$$

where $\phi = \cos^{-1} \left[\dfrac{8}{16 + (Q_s k)^2 L_s/L_p} \right]^{\frac{1}{2}}$.

For many practical cases it will be found sufficiently accurate to take $\tan \phi = 1$ in eqn. (12).

(iii) Electronic reactances

There are a number of forms which electronic reactance circuits may take and a few of these are given below.

(1) **Resistance in series with a capacitance.** This arrangement is shown in Fig. 29.10, but since the circuit imposes severe resistive loading on the oscillator circuit its use is not advised. (See Ref. 10).

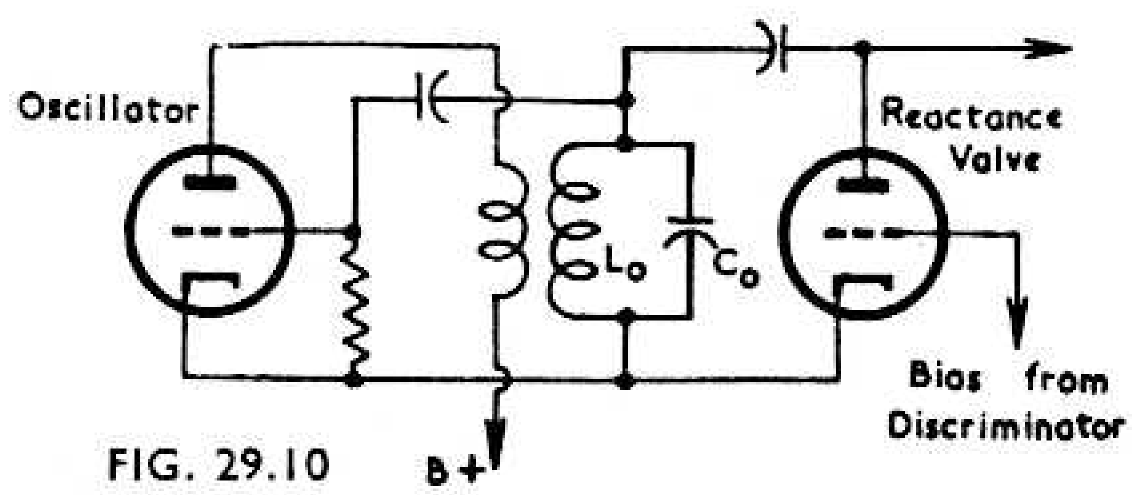

FIG. 29.10

(2) **Miller effect circuits.** These circuits (Fig. 29.11) rely on the change of input capacitance which occurs when the gain is varied. If the plate load can be tuned so that it behaves as a pure resistance, then the valve input resistance can be made very large. For the circuit shown there will be a resistive input component due to Miller effect because of stray capacitance across the load resistor. The application of the circuit is largely confined to use with fixed tuned oscillator circuits.

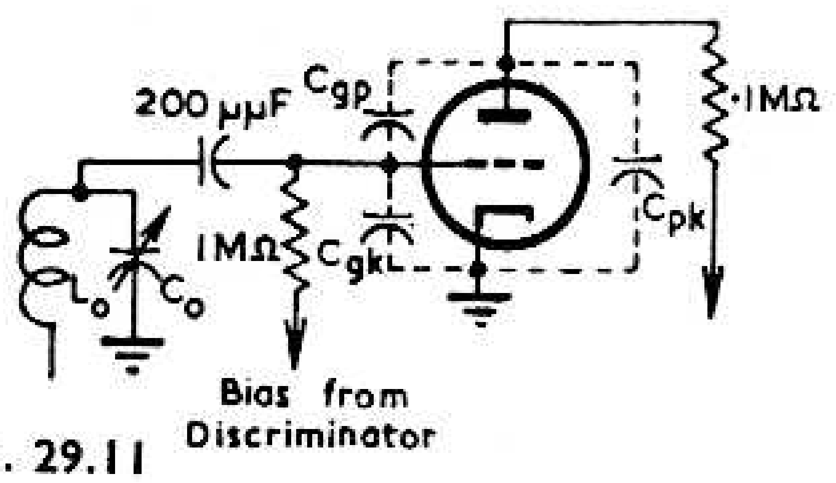

FIG. 29.11

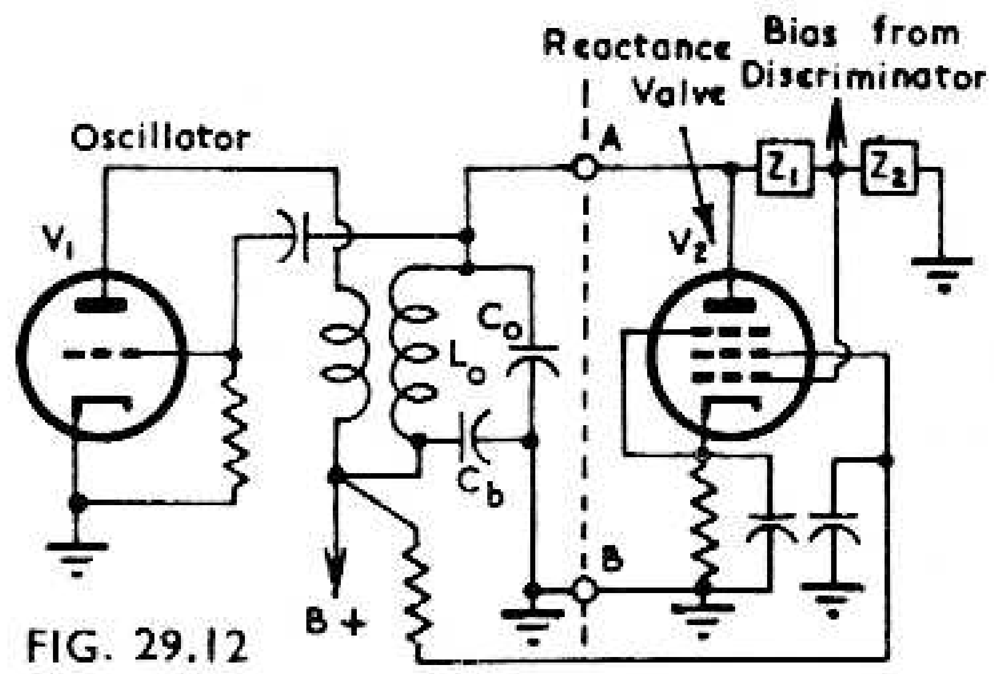

FIG. 29.12

(3) **Quadrature circuits** (Figs. 29.12, 29.13). The grid is fed from a resistance reactance network connected between plate and cathode. This provides a voltage between the grid and cathode which is almost 90° out of phase with the plate to cathode voltage. The source of the alternating plate to cathode voltage is the voltage developed across the tank circuit of the oscillator (see Fig. 29.12). Since the plate current is in phase with the grid voltage (for valves having high plate resistance) the plate voltage and plate current will be approximately 90° out of phase. To the external circuit (oscillator tank circuit in this case) connected between plate and cathode of the reactance valve the behaviour is as though an additional reactance and resistance had been connected in parallel. Whether the valve circuit behaves like an inductive, or a capacitive reactance depends on the resistance-reactance network arrangement, as can be seen from Fig. 29.13.

The value of the apparent reactance and resistance, due to the electronic reactance (more correctly electronic impedance) depends on the mutual conductance (g_m) of the valve, and as the g_m can be controlled by alteration of the grid voltage the equivalent reactance and resistance can also be varied (the resistance variation is usually undesirable). The required grid voltage variation is obtained by utilizing the direct voltage changes at the discriminator output, when the reactance valve is used in a.f.c. circuits. Frequency modulation, using this method, is obtained by applying the audio frequency modulating voltage to the grid of the reactance valve, in the same way as the direct voltage changes are applied for obtaining a.f.c. The magnitude of the a-f voltage determines the change in the equivalent reactance shunted across the oscillator tank circuit, and so determines the frequency deviation from the nominal oscillator centre frequency. The number of times the frequency deviates around the central reference frequency will be determined by the frequency of the a-f modulating voltage. Variation in the value of the shunt resistance, due to the electronic reactance, across the oscillator circuit causes undesired amplitude modulation.

The quadrature circuits are the most widely used for a.f.c. and other purposes, and attention will be confined to discussing some of the possible arrangements. Fig. 29.12 shows the general circuit arrangement using a pentode valve. A hexode or heptode valve can also be used, with the phase shifting network connected to the signal grid and the control voltage to the oscillator grid. The impedances Z_1 and Z_2

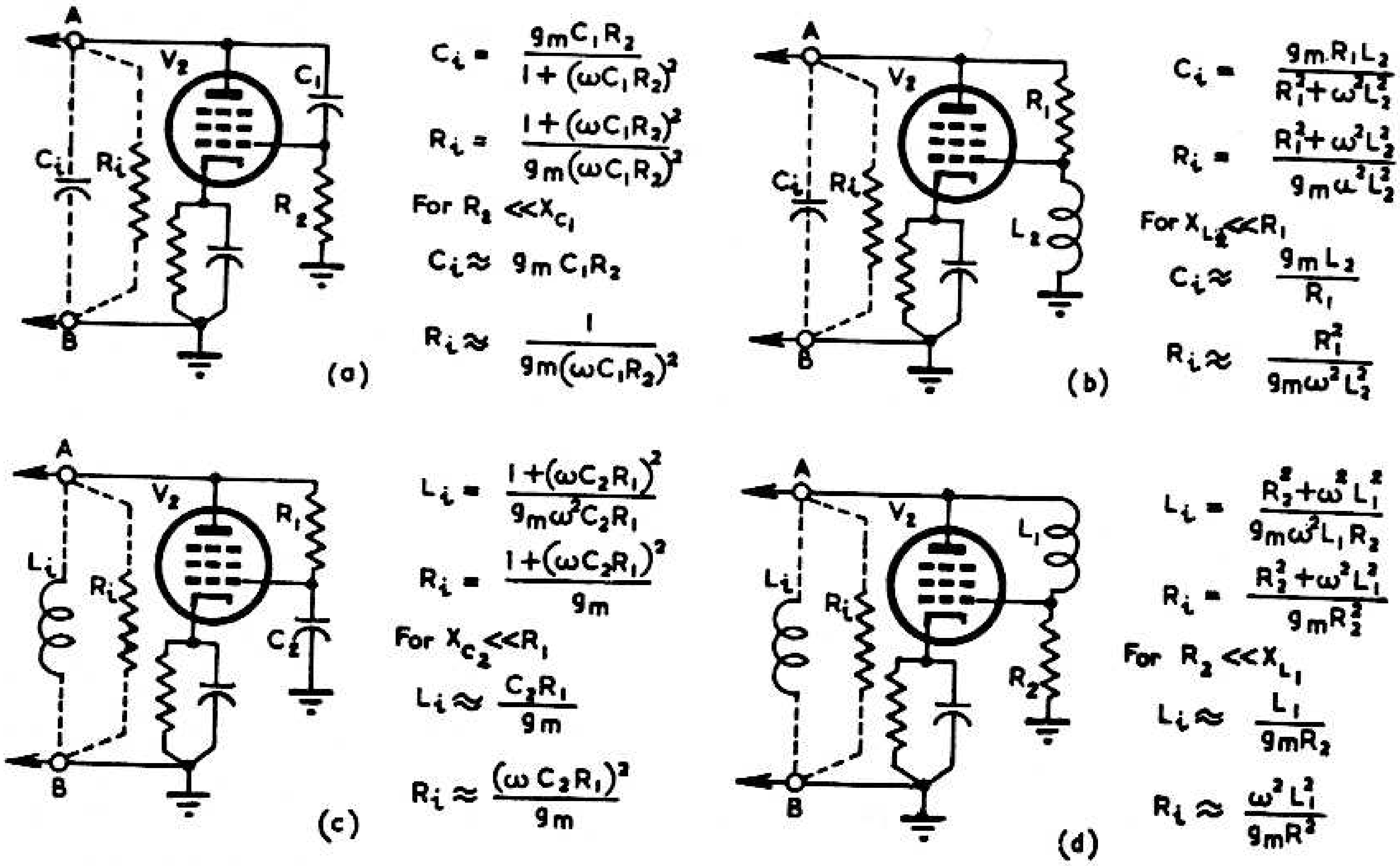

FIG. 29.13

in Fig. 29.12 comprise the phase shifting network. Depending on the form these impedances take it will be clear that an additional blocking capacitor may be required between plate and grid of the reactance valve, and also, since there must be a d.c. path between grid and cathode, an additional grid resistor may be necessary. The values for these additional components should be such as to have negligible effect on the performance of the circuit. Fig. 29.13 shows four possible arrangements for quadrature circuits, together with the equations for the additional resistance (R_i) and inductance (L_i), or capacitance (C_i), connected in parallel with the oscillator tuned circuit. Exact and approximate equations are given, but in most practical circuits the approximate conditions will hold. The equations apply equally well to quadrature circuits using pentode, hexode or heptode valves. The angular frequency ω is that at which the oscillator circuit is meant to operate e.g. $2\pi \times 1455$ Kc/s etc. (in the case of F-M this would be the nominal reference frequency). The circuit of Fig. 29.13(c) is the one most commonly used in practical a.f.c. circuits in which the oscillator is tuned by a variable capacitor. Care is necessary when using circuits (b) and (d) as self resonance effects, due to stray capacitances across the inductances L_2 and L_1, often lead to difficulties. Further, the r-f resistances of L_2 and L_1 must be low if the circuits are to behave as relatively pure reactances. Stray capacitances across R_1 and R_2 can also affect performance, and should be kept small.

To carry out the design for an electronic reactance circuit it is necessary to know the manner in which g_m varies with grid bias. This information is generally available on valve data sheets, for a given set of operating conditions. If other operating conditions are required, then direct measurement of the $g_m - e_g$ characteristic is the usual procedure.

It is helpful when designing reactance valve circuits to be able to determine, directly, values for C_1R_2, L_2/R_1, R_1C_2 and L_1/R_2 in terms of the operating frequency, the frequency change required, and the oscillator tank circuit component values. The necessary conditions have been determined (Ref. 18) for the circuits (b) and (c) of Fig. 29.13, using the approximate relationships for C_i and L_i and assuming that the frequency variation is linear (or very nearly so). For circuit (b) the approximate expression is

$$\frac{L_2}{R_1} = \frac{2C_0 f_2 S}{f_1^{\,2}} \qquad (13)$$

For circuit (c) the approximate expression is

$$C_2R_1 = \frac{L_0f_1^2}{2f_2S} \tag{14}$$

where C_0 = capacitance tuning the oscillator circuit in the absence of the reactance valve

L_0 = inductance of the oscillator tuned circuit in the absence of the reactance valve

S = sensitivity = $(f_2 - f_1)$/corresponding change in mutual conductance (g_m)

f_2 = high frequency limit of frequency

and f_1 = low frequency limit of frequency

The design procedure is as follows :

(1) Select f_2 and f_1. Suppose the nominal oscillator centre frequency is 1455 Kc/s, and the oscillator frequency is to vary $\pm$ 5 Kc/s. Then $f_2 = 1460$ Kc/s and $f_1 = 1450$ Kc/s.

(2) Select a suitable working range on the $g_m - e_g$ characteristics, for the valve type to be used, which is as nearly linear as is possible. With a valve type 6U7-G (250 volts on plate, 100 volts on screen) a suitable operating range is from -3 to -10 volts, giving a g_m change of $1600-275 = 1325$ μmhos.

(3) Choose a suitable value for L_0 or C_0 if these are not already fixed by other circuit considerations. Suppose $L_0 = 110$ μH is required in a typical case ; this value would be modified slightly in the final circuit, to take care of the additional parallel inductive reactance due to the normal value of the electronic reactance in the absence of additional bias from the discriminator. It is not necessary, usually, to take this inductance change into account during the preliminary design.

(4) Compute the sensitivity (S) in cycles per mho. For our example $S = (10$ Kc/s)/1325 μmhos $= 7.54 \times 10^6$ cycles/mho.

(5) Determine L_2/R_1 from eqn. (13) or C_2R_1 from eqn. (14). Using eqn. (14),

$$C_2R_1 = \frac{110 \times 10^{-6} \times 1450^2 \times 10^6}{2 \times 1460 \times 10^3 \times 7.54 \times 10^6} = 10.5\ \mu\mu\text{F} \times \text{M}\Omega$$

(6) Select particular values for L_2, R_1 or C_2 to conform to the circuit requirements ; remembering the previous restrictions of $X_{L_2} \ll R_1$ and $X_{C_2} \ll R_1$.

This should lead to R_1 being at least 5 times X_{L_2} or X_{C_2}, but larger ratios are preferable (see below).

The most convenient procedure is to tabulate various values of R_1, L_2 or C_2 and to select the most suitable combination giving the product found in step (5) e.g. $R_1 = 50\,000\ \Omega = 0.05$ MΩ, then $C_2 = 10.5/0.05 = 210$ $\mu\mu$F, and so $X_{C_2} = 520\ \Omega$. This makes $R_1 \gg X_{C_2}$ as required.

Of course, the actual values of L_i and R_i can be determined directly from the expressions given in Fig. 29.13. R_i should always be so determined for the condition of maximum g_m, after the circuit values have been found, to ensure that the loading on the oscillator circuit is not excessive. The value of g_m to be used in these equations corresponds to the actual bias voltage for a particular operating frequency ; e.g. in the above example, with no additional external bias applied, the operating frequency is 1455 Kc/s, and the standing bias voltage can be taken as -6.5 volts, corresponding to a mutual conductance of 925 μmhos. The total parallel inductance and resistance changes can be found, using the g_m values corresponding to -3 and -10 volts bias, which are the values required when the operating frequencies are 1450 Kc/s and 1460 Kc/s respectively.

Before completing a design it is necessary to check the amplitude of the oscillator voltage applied to the grid of the reactance valve by the phase shifting network. This check is necessary as the possibility of grid current might be overlooked. In our example the minimum bias is −3 volts and so the peak r-f grid voltage should not exceed about 2 volts if grid current is to be avoided. The proportion of the r-f voltage developed across the oscillator tank circuit (and applied between plate and cathode of the reactance valve) which appears between grid and cathode of the reactance valve is for Fig. 29.13(c) $X_{C_2}/\sqrt{X^2_{C_2} + R_1^2}$. For our example, the voltage step down is 0.0104, and so no possibility of grid current exists, as 2 volts peak r-f at the grid corresponds to 196 volts peak across the oscillator tank circuit. This is considerably in excess of the voltage likely to be encountered in a receiver oscillator circuit, where 60 volts peak is about the maximum to be expected with any of the usual arrangements (it is usually considerably less than this value, depending on the type of circuit used).

Further details of the design of reactance valve circuits for a.f.c. can be found in Refs. 8, 9 and 10. A graphical method for determining the "throw-out" and "pull-in" frequencies of an a.f.c. system is given in Ref. 8 (p. 260). The difference in these two frequencies is reduced by using an electronic reactance which gives correction for a limited range of discriminator voltages only ; outside the correction range the added reactance should remain practically constant.

SECTION 3 : REFERENCES

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See also Refs. 40, 41, 42 Chapter 27.

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(Refs. 18-22 are of general interest in the design of F-M test equipment etc.)